Universal High Brightness LED Driver

Halogen Free

General Description

The FP7181 is an open loop, current mode, control LED driver IC. It includes an 10 - 450V linear regulator which allows it to work from a wide range of input voltages without the need for an external low voltage supply. The FP7181 is ideally suited for buck LED drivers. The FP7181 built-in 8Ω power MOSFET makes this regulator highly power efficient.

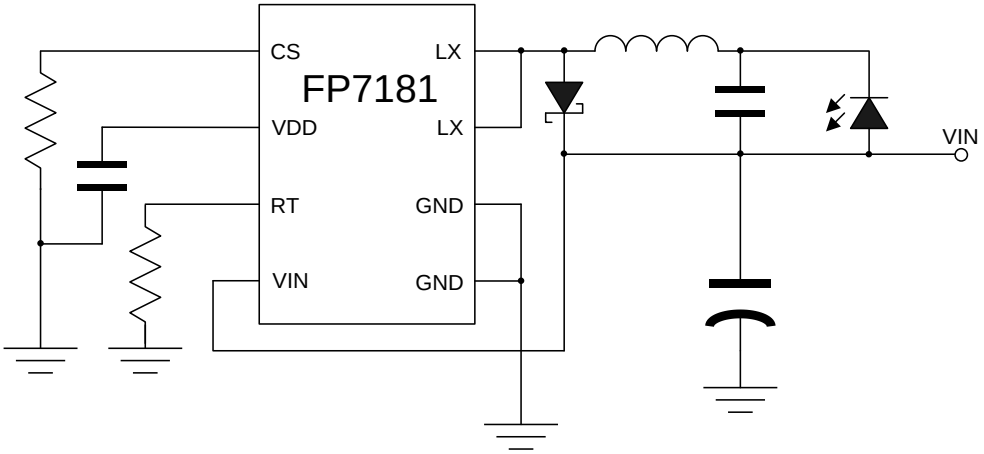
Features

- Switch mode controller for single switch LED drivers
- Enhanced drop-in replacement to the FP7181
- Open loop peak current controller
- Internal 10 to 450V linear regulator
- Requires few external components for operation

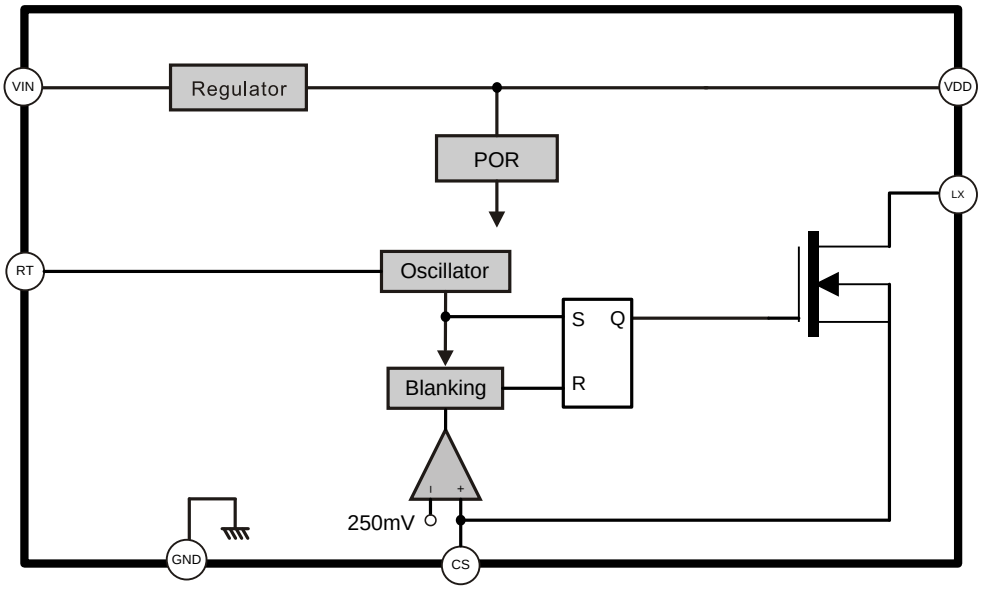
Applications

- DC/DC or AC/DC LED driver applications
- RGB backlighting LED driver
- Back lighting of flat panel displays
- General purpose constant current source
- Signage and decorative LED lighting
- Chargers

Typical Application Circuit

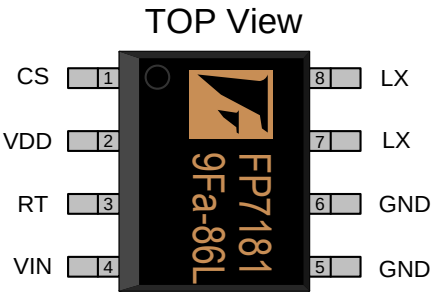


Function Block Diagram



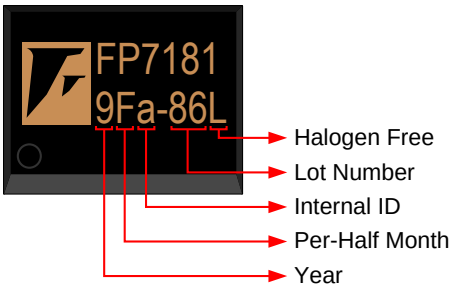
Pin Descriptions

SOP-8L



Name	No.	I / O	Description
CS	1	I	This pin is the current sense pin used to sense the FET current by means of an external sense resistor.
VDD	2	I	This is the power supply pin for all internal circuits.
RT	3	I	This pin sets the oscillator frequency.
VIN	4	I	This pin is the input of an 10 - 450V linear regulator
GND	5	P	Ground return for all internal circuitry.
GND	6	P	Ground return for all internal circuitry.
LX	7	O	Power Switch Output
LX	8	O	Power Switch Output

Marking Information



Halogen Free: Halogen free product indicator

Lot Number: Wafer lot number's last two digits

For Example: 132386TB → 86

Internal ID: Internal Identification Code

Per-Half Month: Production period indicated in half month time unit

For Example: January → A (Front Half Month), B (Last Half Month)

February → C (Front Half Month), D (Last Half Month)

Year: Production year's last digit

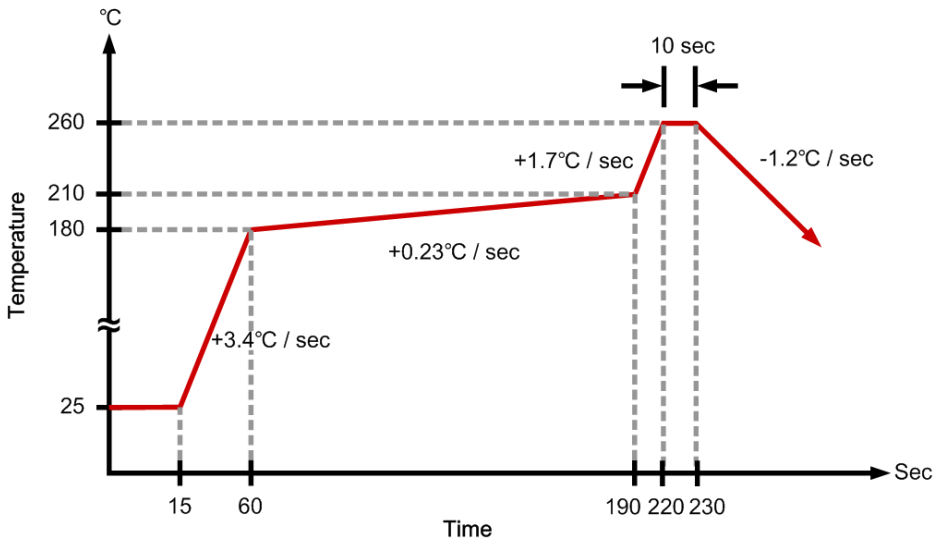
Ordering Information

Part Number	Operating Temperature	Package	MOQ	Description
FP7181DR-G1	-25°C ~ +85°C	SOP-8L	2500 EA	Tape & Reel

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{IN}	V_{IN} to GND			470	V
	VDD	VDD to GND			8	V
LX					600	V
CS, RT			-0.3		V_{DD}-0.3V	V
Allowable Power Dissipation	P_D	SOP-8L $T_A \leqq +25°C$			630	mW
Junction to Ambient Thermal Resistance	θ_{JA}			128		°C / W
Junction Temperature	T_J				+125	°C
Operating Temperature			-25		+85	°C
Storage Temperature	T_S	SOP-8L	-40		+150	°C
SOP-8L Lead Temperature		(soldering, 10 sec)			+260	°C

IR Re-flow Soldering Curve



Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}		10		450	V
Operating Temperature Range	T_A		-25		85	°C

DC Electrical Characteristics (V_{CC}=10V,T_A = 25°C, unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Internal Regulator						
Internally regulated voltage	V_{DD}	VIN = 10V, $I_{DD(ext)}$= 0, RT=226kΩ	7.25	7.5	7.75	V
Line regulation of VDD	Δ V_{DD}	VIN = 10 – 450V, $I_{DD(ext)}$=0, R =226kΩ	0	-	1.0	V
Internal Regulator						
Load regulation of V_{DD}	Δ $V_{DD,load}$	$I_{DD(ext)}$ = 0 - 1.0mA, 500pF at GATE; RT = 226kΩ	0		100	mV
V_{DD} undervoltage lockout threshold	UVLO	V_{DD} rising	6.45	6.7	6.95	V
V_{DD} undervoltage lockout hysteresis	Δ UVLO	V_{DD} falling		500		mV
Current Sense Comparator						
Current sense pull-in threshold voltage	$V_{CS,TH}$	-25°C < T_A < +85°C	225	250	275	nV
		T_A < +125°C	213	250	287	
Current sense blanking interval	T_{BLANK}	0 < T_A < +85°C, V_{CS} =$V_{CS,TH}$ + 50mV after T_{BLANK}	150	215	280	ns
		-25 < T_A < +125°C, V_{CS} = $V_{CS,TH}$ + 50mV after T_{BLANK}	145	215	315	
Delay to output	t_{DELAY}			80	150	ns
Oscillator						
Oscillator frequency	f_{OSC}	R_T = 1.00MΩ	20	25	30	kHz
		R_T = 226kΩ	80	100	120	

Function Description

Input Voltage Regulator

The FP7181 can be powered directly from its VIN pin and can work from 10 - 450VDC at its VIN pin. When a voltage is applied at the VIN pin, the FP7181 maintains a constant 7.5V at the VDD pin. This voltage is used to power the IC and any external resistor dividers needed to control the IC. The VDD pin must be bypassed by a low ESR capacitor to provide a low impedance path for the high frequency current of the output GATE driver.

The FP7181 can also be operated by supplying a voltage at the VDD pin greater than the internally regulated voltage. This will turn off the internal linear regulator of the IC and the FP7181 will operate directly off the voltage supplied at the VDD pin. Please note that this external voltage at the VDD pin should not exceed 8V.

Although the VIN pin of the FP7181 is rated up to 450V, the actual maximum voltage that can be applied is limited by the power dissipation in the IC. For example, if an 8-pin SOIC (junction to ambient thermal resistance Rθ,j-a = 128°C/ W) FP7181 draws about I_{IN} = 2.0mA from the VIN pin, and has a maximum allowable temperature rise of the junction temperature limited to about ΔT = 100°C, the maximum voltage at the VIN pin would be:

$$V_{IN(MAX)} = \frac{\Delta T}{R_{\theta,j-a}} \cdot \frac{1}{I_{in}} = \frac{100^{o}C}{128^{o}C/W} \cdot \frac{1}{2mA} = 390V$$

In these cases, to operate the FP7181 from higher input voltages, a Zener diode can be added in series with the VIN pin to divert some of the power loss from the FP7181 to the Zener diode. In the above example, using a 100V zener diode will allow the circuit to easily work up to 450V.

The input current drawn from the VIN pin is a sum of the 1.0mA current drawn by the internal circuit and the current drawn by the GATE driver (which in turn depends on the switching frequency and the GATE charge of the internal FET).

$$I_{IN} \approx 1.0mA + Q_G \cdot f_S$$

In the above equation, f_S is the switching frequency and QG is the GATE charge of the internal FET (which can be obtained from the datasheet of the FET).

Current Sense

The current sense input of the FP7181 goes to the noninverting inputs of two comparators. The inverting terminal of one comparator is tied to an internal 250mV reference. The outputs of the comparators also include a 150-280ns blanking time which prevents spurious turn-offs of the internal FET due to the turn-on spike normally present in peak current mode control. In rare cases, this internal blanking might not be enough to filter out the turn-on spike. In these cases, an external RC filter needs to be added between the external sense resistor (R_{CS}) and the CS pin.

Please note that the comparators are fast (with a typical 80ns response time). Hence these comparators are more susceptible to be triggered by noise than the comparators of the FP7181. A proper layout minimizing external inductances will prevent false triggering of these comparators.

Oscillator

The oscillator in the FP7181 is controlled by a single resistor connected at the RT pin. The equation governing the oscillator time period t_{OSC} is given by:

$$t_{OSC}(us) = \frac{R_T(k\Omega)}{20.7}$$

If the resistor is connected between RT and GND, FP7181 operates in a constant frequency mode and the above equation determines the time-period.

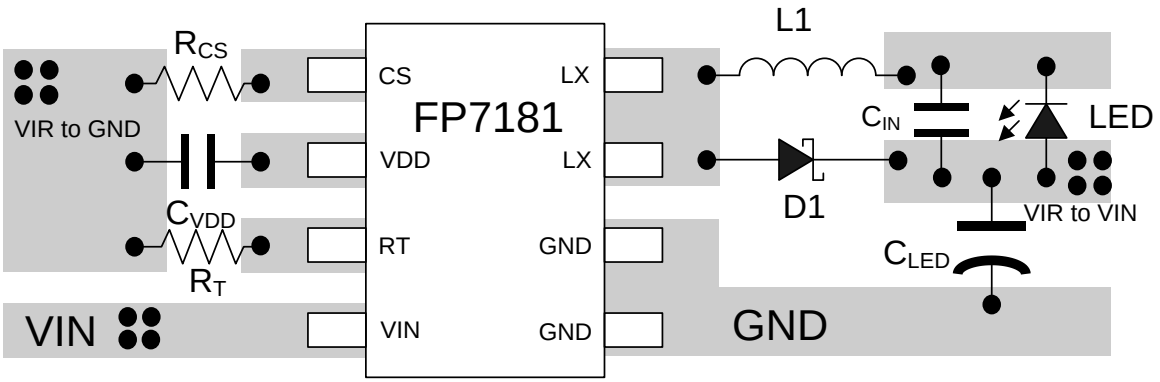
Application Information

The FP7181 is optimized to drive buck LED drivers using open-loop peak current mode control. This method of control enables fairly accurate LED current control without the need for high side current sensing or the design of any closed loop controllers. The IC uses very few external components.

A resistor connected to the RT pin programs the frequency of operation. The oscillator produces pulses at regular intervals. These pulses set the SR flip-flop in the FP7181 which causes the GATE driver to turn on. The same pulses also start the blanking timer which inhibits the reset input of the SR flip flop and prevent false turn-offs due to the turn-on spike. When the FET turns on, the current through the inductor starts ramping up. This current flows through the external sense resistor R_{CS} and produces a ramp voltage at the CS pin. The comparators are constantly comparing the CS pin voltage to the internal 250mV. Once the blanking timer is complete, the output of these comparators is allowed to reset the flip flop. When the output of either one of the two comparators goes high, the flip flop is reset and the GATE output goes low. The GATE goes low until the SR flip flop is set by the oscillator. Assuming a 30% ripple in the inductor, the current sense resistor R_{CS} can be set using:

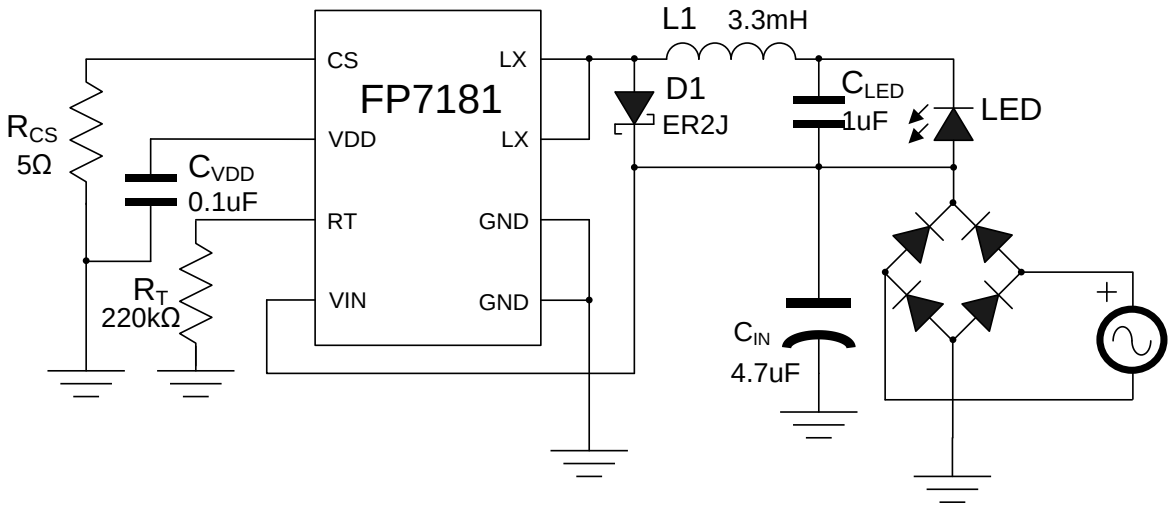
$$R_{CS} = \frac{0.25V}{1.15 \cdot I_{LED}(A)}$$

Constant frequency peak current mode control has an inherent disadvantage – at duty cycles greater than 0.5, the control scheme goes into subharmonic oscillations. To prevent this, an artificial slope is typically added to the current sense waveform. This slope compensation scheme will affect the accuracy of the LED current in the present form. However, a constant off-time peak current control scheme does not have this problem and can easily operate at duty cycles greater then 0.5 and also gives inherent input voltage rejection making the LED current almost insensitive to input voltage variations. But, it leads to variable frequency operation and the frequency range depends greatly on the input and output voltage variation. FP7181 makes it easy to switch between the two modes of operation by changing one connection (see oscillator section).



Suggested Layout

Typical Application

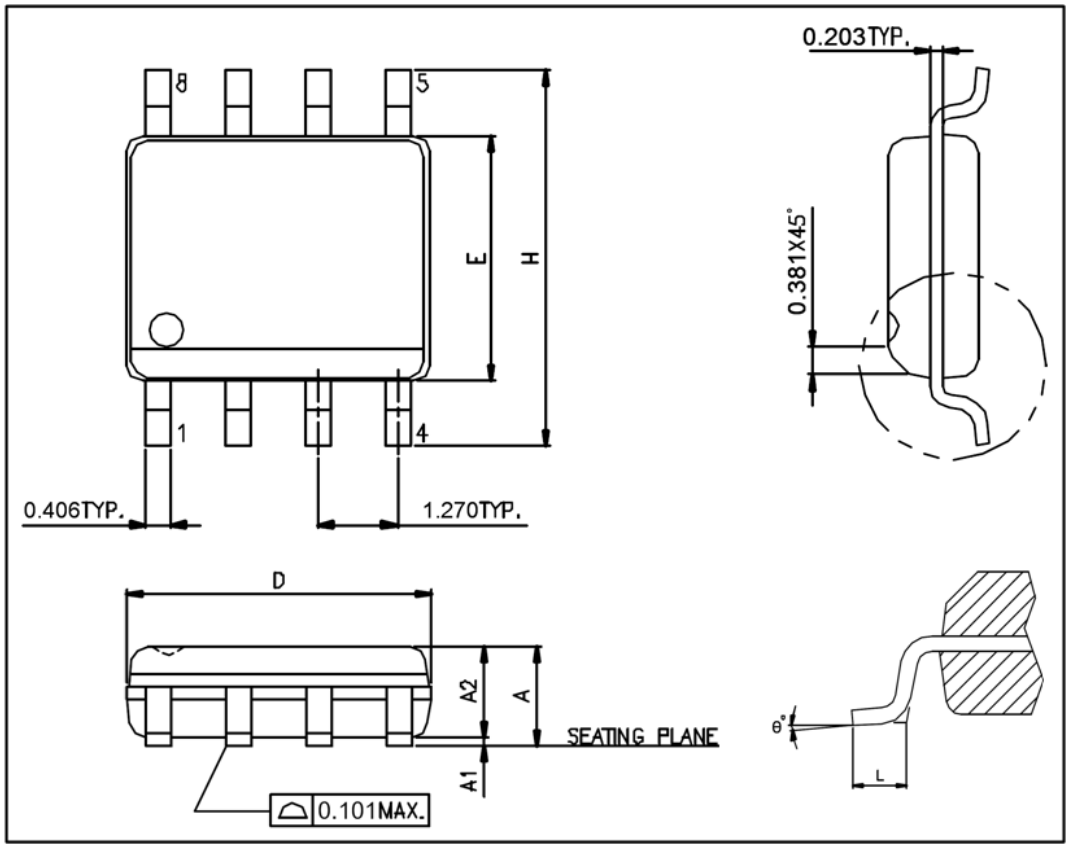


Notice:

1. **Tapping reel aluminum foil bags after unpacking must be stored at ≤10% RH environment.**
2. **Tapping reel aluminum foil bags after unpacking must sure surface-mount is completed within 168 hours.**

Package Outline

SOP-8L



UNIT: mm

Symbols	Min. (mm)	Max. (mm)
A	1.346	1.752
A1	0.101	0.254
A2		1.498
D	4.800	4.978
E	3.810	3.987
H	5.791	6.197
L	0.406	1.270
θ°	0°	8°

Note:

1. Package dimensions are in compliance with JEDEC Outline: MS-012 AA.
2. Dimension “D” does not include molding flash, protrusions or gate burrs.
3. Dimension “E” does not include inter-lead flash, or protrusions.